WHAT IS CLAIMED IS:

1. A testing card, which is used to be coupled to a card interface installed in an electronic device to test a function of the card interface, wherein the card interface complies with an interface specification, and the testing card comprises:

a converting circuit which is used to receive, convert and output an attribute control signal, a common memory signal and an I/O signal fed in from the card interface;

a latch circuit which is used to receive a data signal fed in from the card interface, latch the data signal and have the data signal outputted afterwards;

a data processor, which is coupled to the converting circuit and the latch circuit and is used to proceed with testing according to the data signal and the signal outputted from the converting circuit;

a signal generator which is used to output a mode selection signal and an interrupt signal to the card interface, generate and output an enable signal according to a control signal fed in from the card interface;

an oscillation combination circuit, which is coupled to the signal generator and is used to generate a wait signal according to the enable signal and feed the wait signal into the card interface; and

a reset circuit, which is coupled to the latch circuit, the data processor, the signal generator and the oscillation combination circuit and is used to reset the above latch circuit, the data processor, the signal generator and the

oscillation combination circuit.

2. The testing card according to claim 1, wherein the electronic device is a personal digital assistant.

3. The testing card according to claim 2, wherein the personal digital assistant adopts WinCE operating system.

4. The testing card according to claim 1, wherein the interface is of personal computer memory card international association specification (PCMCIA specification).

5. The testing card according to claim 1, wherein the interface is of compact flash specification (CF specification).

6. The testing card according to claim 1, wherein the data processor is a flash memory.

7. The testing card according to claim 1, wherein the enable signal is a negative trigger signal.

8. The testing card according to claim 1, wherein the wait signal is a square-wave signal.

9. The testing card according to claim 1, wherein the testing method performed by the testing card comprises the steps of:

identifying the testing card: displaying an error message if identification

fails, otherwise proceeding with step A;

A. proceeding with 16 bits I/O addressing mode test: displaying an error message if the test fails, otherwise proceeding with step B;

B. proceeding with 16 bits attribute addressing mode test: displaying an error message if the test fails, otherwise proceeding with step C;

C. proceeding with memory addressing mode test: displaying an error message if the test fails, otherwise proceeding with step D;

D. setting the test to be 8 bits testing mode;

E. proceeding with 8 bits I/O addressing mode test: displaying an error message if the test fails, otherwise proceeding with step F;

F. enabling the wait signal and executing counting;

G. disabling the wait signal and executing counting; and

determining if the wait signal complies with the standard value according to the values of counting obtained in step F and step G respectively: if no, displaying an error message; if yes, concluding the testing process.

10. The testing card according to claim 9, wherein the enable signal is a negative trigger signal.

11. The testing card according to claim 9, wherein the wait signal is a square-wave signal.

12. A testing method which uses a testing card to test functions of a card interface, wherein the testing method comprises the steps of:

identifying the testing card: displaying an error message if identification

fails, otherwise proceeding with step A;

A. proceeding with 16 bits I/O addressing mode test: displaying an error message if the test fails, otherwise proceeding with step B;

B. proceeding with 16 bits attribute addressing mode test: displaying an error message if the test fails, otherwise proceeding with step C;

C. proceeding with 16bits memory addressing mode test: displaying an error message if the test fails, otherwise proceeding with step D;

D. setting the test to be 8 bits testing mode;

E. proceeding with 8 bits I/O addressing mode test: displaying an error message if the test fails, otherwise proceeding with step F;

F. enabling the wait signal and executing counting;

G. disabling the wait signal and executing counting; and

determining if the wait signal complies with the standard value according to the values of counting obtained in step F and step G respectively: if no, displaying an error message; if yes, concluding the testing process.

13. The testing method according to claim 12, wherein the enable signal is a negative trigger signal.

14. The testing method according to claim 12, wherein the wait signal is a square-wave signal.

15. A testing system, coupled to a card interface installed in an electronic device to test a function of the card interface, wherein the card interface complies with an interface specification, the testing system comprising:

a converting circuit which is used to receive, convert and output an attribute control signal, a common memory signal and an I/O signal fed in from the card interface;

a latch circuit which is used to receive a data signal fed in from the card interface, latch the data signal and have the data signal outputted afterwards;

a data processor which is coupled to the converting circuit and the latch circuit and is used to proceed with testing according to the data signal and the signal outputted from the converting circuit, wherein the data processor will perform testing system identification when the card interface is inserted into the testing system: displaying an error message if the identification fails, otherwise proceeding with step A if the identification is successful;

A. proceeding with 16 bits I/O addressing mode test of the I/O signal: displaying an error message if the test fails, otherwise proceeding with step B;

B. proceeding with 16 bits attribute addressing mode test of the control signal: displaying an error message if the test fails, otherwise proceeding with step C;

C. proceeding with 16 bits memory addressing mode test of the common memory signal: displaying an error message if the test fails, otherwise proceeding with step D;

D. setting the test to be 8 bits testing mode;

E. proceeding with 8 bits I/O addressing mode test of the I/O

signal and displaying an error message if the test fails;

a signal generator which is used to output a mode selection signal and an interrupt signal to the card interface, and, according to a control signal fed in from the card interface, generate an enable signal and have the enable signal outputted afterwards;

an oscillation combination circuit, which is coupled to the signal generator and is used to generate a wait signal according to the enable signal and feed the wait signal to the card interface, wherein the oscillation combination circuit outputs the wait signal according to the enable signal to execute counting processing, and, after the counting is finished, the wait signal is disabled and the counting processing is executed again, and wherein the data processor determines if the wait signal complies with the standard according to the values of counting obtained when the wait signal is enabled and disabled respectively; and

a reset circuit, which is coupled to the latch circuit, the data processor, the signal generator and the oscillation combination circuit and is used to reset the above latch circuit, the data processor, the signal generator and the oscillation combination circuit.

16. The testing system according to claim 15, wherein the electronic device is a personal digital assistant.

17. The testing system according to claim 15, wherein the personal digital assistant adopts WinCE operating system.

18. The testing system according to claim 15, wherein the enable signal is a negative trigger signal.

19. The testing system according to claim 15, wherein the wait signal is a square-wave signal.

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